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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/800,240	MAY ET AL.	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 3 is objected to because of the following informalities: It appears that the word "the" was accidentally inserted between "with" and "one" in line 2 of claim 3. Appropriate correction is required.

Claims 8 and 9 are objected to because of the following informalities: It appears that duplicate copies of claims 8 and 9 were supplied. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 12-14, 17-19, 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Shimotono, US Patent no. 6,509,911.

Regarding claims 12, 14, 17, 24 and 25, Shimotono discloses a device comprising:

a first circuit operable in a first clock domain [CPU in Figure 2 and column 3, lines 52-62];

a first communication media coupled to the first circuit and configured to transfer information [FSB in Figure 2 and column 3, lines 52-62];

a second circuit operable in a second clock domain [Cardbus Controller in Figure 2 and column 4, lines 33-40];

a second communication media coupled to the second circuit and the first communication media, wherein the second communication media configured to transfer information [PCI bus in Figure 2 and column 4, lines 33-40; and

a communication circuit coupled to the first and second communication medium and configured to provide communication between the first and second circuits [Memory/PCI Control Chip in Figure 2 and column 4, lines 3-8].

Regarding claim 13, Shimotono, as described above, discloses that the device includes a CPU, which is an integrated circuit with a plurality of circuits deposited thereon.

Regarding claim 18, Shimotono further discloses that the information may be data [column 3, line 59 - column 4, line 7].

Regarding claim 19, Shimotono further discloses that the information may be control signals [column 3, line 59 - column 4, line 7].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimotono, US Patent no. 6,509,911, in view of Rao, US Patent no. 6,173,356 and Cliff et al., US Patent no. 6,271,681 [Cliff].

Regarding claims 1 and 2, Shimotono discloses a digital system integrated on a semiconductor chip, comprising:

a first circuit [CPU in Figure 2] coupled to a first bus [FSB in Figure 2] in a first clock domain [column 3, lines 52-62];

a second circuit [Cardbus Controller in Figure 2] coupled to a second bus [PCI Bus in Figure 2] in a second clock domain [column 4, lines 33-40];

a first bridge [Memory/PCI Control Chip in Figure 2] in between the first and second buses operable to de-couple the first clock domain from the second clock domain [column 4, lines 3-8].

Shimotono does not disclose that the first circuit [CPU] coupled to the first bus is a bus master. However, as shown by Rao, using a CPU as a bus master for a system is well known in the art [column 5, lines 63-67]. It would have been obvious to one of ordinary skill in the art to use the Shimotono CPU as a bus master to control communication between components in the system.

Shimotono and Rao do not disclose that the second circuit [Cardbus Controller] coupled to the second bus [PCI bus] is a programmable logic device. Cliff discloses using PCI bus compatible programmable logic devices in a system in order to take advantage of the ability of programmable logic devices to be reprogrammed to perform a variety of functions [column 7, line 63 – column 8, line 34]. It would have been obvious to one of ordinary skill in the art to

modify the Shimotono and Rao system to include a programmable logic device coupled to the PCI bus. One of ordinary skill in the art would be motivated to add a PCI bus compatible programmable logic device to the system in order to add functionality to the system by taking advantage of the ability of programmable logic devices to be reprogrammed to perform a variety of functions.

Regarding claim 3, Cliff further discloses that the PCI bus compatible programmable logic device may assume the role of a PCI bus slave [column 8, lines 5-9].

Regarding claim 4, Cliff further discloses that the PCI bus compatible programmable logic device may assume the role of a PCI bus master [column 8, lines 5-9].

Regarding claim 5, Cliff further discloses that the PCI bus compatible programmable logic device may act as an interface between components in the system [column 8, lines 27-34].

Regarding claim 6, Shimotono, Rao and Cliff do not disclose a plurality of second bus masters coupled to the second bus. Examiner takes official notice that coupling a plurality of bus masters to a PCI bus is well known in the art. It would have been obvious to one of ordinary skill in the art to add a plurality of bus masters to the Shimotono, Rao and Cliff system to share the load of handling PCI bus requests.

Claims 7, 8, 10, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimotono, US Patent no. 6,509,911, in view of Cliff et al., US Patent no. 6,271,681 [Cliff].

Regarding claim 7, Shimotono discloses a digital system on a semiconductor chip, comprising:

a central processing unit (CPU) coupled to a first bus [FSB in Figure 2 and column 3, lines 52-62];

a second circuit [Cardbus Controller in Figure 2] coupled to a second bus [PCI Bus in Figure 2] in a second clock domain [column 4, lines 33-40]; and

a bus bridge coupled between the first and second buses [Memory/PCI Control Chip in Figure 2 and column 4, lines 3-8].

Shimotono does not disclose that the second circuit [Cardbus Controller] coupled to the second bus [PCI Bus] is a programmable logic device. Cliff discloses using PCI bus compatible programmable logic devices in a system in order to take advantage of the ability of programmable logic devices to be reprogrammed to perform a variety of functions [column 7, line 63 – column 8, line 34]. It would have been obvious to one of ordinary skill in the art to modify the Shimotono system to include a programmable logic device coupled to the PCI bus. One of ordinary skill in the art would be motivated to add a PCI bus compatible programmable logic device to the system in order to add functionality to the system by taking advantage of the ability of programmable logic devices to be reprogrammed to perform a variety of functions.

Regarding claim 8, Shimotono further discloses that the first bus operates within a first clock domain and the second bus operates within a second clock domain [column 4, lines 3-9].

Regarding claim 10, Shimotono and Cliff do not disclose that the either or both of the FSB and PCI bus operating frequencies are programmable. Examiner takes official notice that systems with programmable FSB or PCI bus speeds are well known in the art. It would have been obvious to one of ordinary skill in the art to modify the Shimontono and Cliff system to

include a programmable FSB or PCI bus operating frequency in order to increase system flexibility.

Regarding claim 20, Shimotono, as described above, discloses a second circuit coupled to a second communication media. Shimotono does not disclose that the second circuit [Cardbus Controller] coupled to the second bus [PCI Bus] is a programmable logic device. Cliff discloses using PCI bus compatible programmable logic devices in a system in order to take advantage of the ability of programmable logic devices to be reprogrammed to perform a variety of functions [column 7, line 63 – column 8, line 34]. It would have been obvious to one of ordinary skill in the art to modify the Shimotono system to include a programmable logic device coupled to the PCI bus. One of ordinary skill in the art would be motivated to add a PCI bus compatible programmable logic device to the system in order to add functionality to the system by taking advantage of the ability of programmable logic devices to be reprogrammed to perform a variety of functions.

Regarding claim 21, Cliff further discloses that the programmable logic device includes a plurality of logic cells having at least one programmable circuit arranged in a multiple dimensional array and at least one interconnector coupled to the plurality of the logic cells and configured to transfer information between the plurality of the logic cells [column 2, lines 30-67].

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimotono, US Patent no. 6,509,911 and Cliff et al., US Patent no. 6,271,681 [Cliff], in view of Van Gaasbeck, US Patent no. 6,434,636.

Regarding claim 9, Shimotono and Cliff are silent as to which of the PCI bus and FSB operates at a greater frequency. However, as shown by Van Gaasbeck, conventional computer systems, at the time of the invention, had FSB speeds greater than 100 MHz and PCI bus speeds of 33-66 Mhz [column 2, lines 25-30]. It would have been obvious to one of ordinary skill in the art to set the FSB and PCI bus frequencies to be consistent with those of conventional FSB and PCI buses to increase system compatibility.

Claims 15, 16, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimotono, US Patent no. 6,509,911

Regarding claims 15, 16 and 22, Shimotono and Cliff do not disclose that the either or both of the FSB and PCI bus operating frequencies are programmable. Examiner takes official notice that systems with programmable FSB or PCI bus speeds are well known in the art. It would have been obvious to one of ordinary skill in the art to modify the Shimontono and Cliff system to include a programmable FSB or PCI bus operating frequency in order to increase system flexibility.

Regarding claim 23, Shimotono and Cliff are silent as to the frequencies pf the FSB and PCI bus. However, it would have been obvious to one of ordinary skill in the art to program the FSB and PCI bus frequencies to be the same in order to facilitate data transmission between the two buses.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v.*

Eagle Mfg. Co., 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claims 1-11 and 20-21 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-12 and 20 of prior U.S. Patent No. 6,745,369. This is a double patenting rejection.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 12-19 and 22-25 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 12-19 and 21-24 of U.S. Patent No. 6,745,369. Although the conflicting claims are not identical, they are not patentably distinct from each other. The limitation, "a programmable logic device operable in a second clock

domain" claimed in claim 12 of U.S. Patent No. 6,745,369, anticipates the limitation "a second circuit operable in a second clock domain" claimed in pending claim 12 because a programmable logic device is a type of circuit. Therefore, claims 12-19 and 21-24 of U.S. Patent No. 6,745,369 and pending claims 12-19 and 22-25 are not patentably distinct from each other.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mergard et al., US Patent no. 6,415,348, discloses a PCI bus with a plurality of bus masters.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
April 6, 2006

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